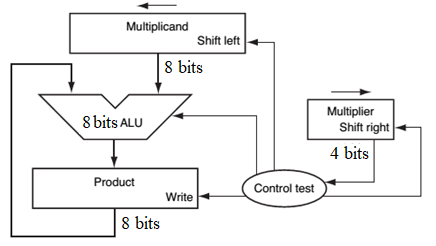
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| UNIVERSITY OF INFOMATION TECH.  **FACULTY OF COMPUTER ENGR.** | **MIDTERM TEST – SEM. I (2018-2019)**  **DIGITAL LOGIC DESIGN**  *DURATION: 90 minutes*  *(Students are* ***allowed*** *to use any documents, but not electronic devices.)* |

1. Given the following state/output table: (5 đ)

|  |  |  |  |
| --- | --- | --- | --- |
| Present State | Next State/Output | | |
| AB = 00 | AB = 01 | AB = 10 |
| S0 | S4/1 | S2/0 | S1/1 |
| S1 | S2/0 | S5/1 | S4/1 |
| S2 | S1/1 | S0/0 | S3/1 |
| S3 | S2/0 | S5/1 | S4/1 |
| S4 | S0/0 | S5/1 | S1/1 |
| S5 | S2/0 | S4/1 | S2/1 |

1. Minimize the states for the above FSM (1 đ)
2. Drive state encoding using the minimum-bit-change heuristic (1 đ)
3. Draw FSM diagram using Moore model (1 đ)
4. Design circuit using Moore model (2 đ)
5. Design a 4x4 register file with two write ports and two read ports. (3đ)
6. Given the circuit of the 4-bit multiplication as following



Using FSM, design the Control test module (3 đ)

**Approved by Head of Subject Designed by**